Reliability Evaluation of Voltage Controlled Oscillators Based On a Device Degradation Sub-Circuit Model

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Abstract **—This paper presents a method for circuit reliability evaluation. Based on the study of device reliability, a sub-circuit describing the device degradation after high-voltage stress is proposed. This model allows circuit reliability of VCOs to be evaluated and provides higher degree of freedom for circuit designers.**

I. INTRODUCTION

Advance VLSI technology has made CMOS more practical and realizable to Ratio-Frequency applications [1]. Most reliability studies of CMOS IC remain in the transistor level [2]. In recent years, a few reports discussing the reliability evaluation in circuit level emerge [3,4,5]. This studies especially focus on analog circuit since its biasing and operation condition are unique. Among various building blocks in RF applications, Voltage Controlled Oscillator (VCO) is widely used in phase-locked-loops, voltage to frequency converters and frequency synthesizer [6,7].

In this paper, we propose a new sub-circuit model for describing device degradation as a function of time and stress. Two VCOs structures, LC-based VCO and PMOS-loaded VCO, are evaluated for its reliable robustness by the simulated degradation, such as oscillation frequency, gain, peak-to-peak output voltage, tuning range and phase noise. This analysis allows us to compare the reliability strength of various circuits and offers the designers additional room in determining tradeoffs between circuit reliability and performance.

II. EXPERIMENT AND THE STRESS MODEL

The schematic plot in Fig. 1 is our proposed sub-circuit model describing device degradation after high-voltage stress. The device's degradation is modeled by two external resistances R_{SS} and R_{GD}. R_{SS} models the degradation of drain current due to mobility reduction after stress, whereas R_{GD} models the stress induced gate oxide leakage current which causes large leakage current between gate and drain during normal operation. This model could predict device degradation as a function of stress voltage and stress time. The device models and circuit design are based on 0.18μm CMOS technology.

The gate voltages are raised to high voltage for accelerated FN stress. Sample transistors are measured under various stress conditions and device characteristics degradation was monitored during stress. During stress, reduction in drain current and a leakage path between gate and drain are observed.

The drain current extracted is modeled by a resistance R_{SS}. R_{SS} is using the ratio of fresh current to stressed current as in Eq. (1).

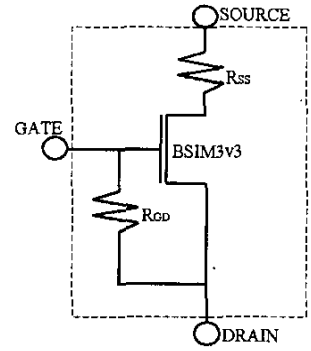

Fig. 1. The sub-circuit model with two additional resistances R_{SS} and R_{GD} for device degradation modeling.

$$R_{ss} = \frac{1}{I(stressed)}(V_{gs} - V_t)\left(1 - \sqrt{\frac{I(stressed)}{I(fresh)}}\right) \quad \text{Eq.(1)}$$

Since R_{GD} expresses the leakage current from the gate oxide to drain, its value can be easily obtained as $R_{GD}=V_{GD}/I_{GD}$ (stressed).

Fig. 2(a) and Fig. 2(b) show the extracted R_{SS} and R_{GD} resistances respectively from the experimental data under different stress voltages. Good agreements are demonstrated between the experimental models of R_{SS} and R_{GD}.

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Fig. 3 compares the fresh and stressed measurement results with the simulated results. The solid squares and the hollow circles represent the measured data of the fresh and the stress devices respectively. A fairly good agreement between the measured data and I-V simulated by the sub-circuit model is demonstrated.

III. EVALUATION CURCUITS

Two VCO configurations for reliability evaluation using the proposed stress model are investigated. The two most commonly used VCO discussed here are LC-based VCO and PMOS-loaded VCO.

In the LC-based VCO, in Fig. 4(a), the MOSFETs, Mn1, Mn2, Mp1 and Mp2, generate negative resistance to compensate LC tank effective positive resistance. Oscillation frequency is tuned by the capacitance changing of varactor. The total transconductance G_m must satisfy [8] to ensure oscillation,

$$G_m > 2G_{tank},$$

where $G_m = g_{m12} + g_{m34}$.

The PMOS-loaded VCO used for our analysis is shown in Fig. 4(b). Four-stage PMOS-loaded ring oscillator is implemented by simply configuring one stage such that it does not invert. The Mp3, Mp4 are biased in deep triode region serving as the load. The control voltage |Vt-Vdd| must be set to define the on-resistance accurately.

Fig. 5 shows the comparison of oscillation frequency with control voltage between LC-based VCO and PMOS-loaded VCO. The center oscillation frequency is designed at around 5.2GHz. The LC-based VCO tuning range is about 1GHz whereas the PMOS-loaded VCO 1.6GHz. The LC-based VCO has a narrower tuning range 18% compared to the PMOS-loaded VCO's tuning range of 29% which is limited by the capacitance of the varactor available in 0.18μm CMOS technology.

IV. FAILURE ANALYSIS

Fig. 6(a) shows the G_m degradation of LC-based VCO. When V_{DD}=5V, operating for 10^5sec, G_m degrades to 13.7m reaching the critical condition for failure to oscillate, $g_{m12}+g_{m34}<2G_{tank}$. With V_{DD} at 4V, the VCO lifetime (define when VCO stops to oscillate) is extended to 10^8sec which is ten year. Fig. 6(b) shows the gain per stage degradation of four-stage PMOS-loaded VCO. For each stage to oscillate, each stage must contribute a phase-shift of 45 degree and hence minimum voltage gain must larger than 1.4. Once the gain per stage is less than 1.4, the VCO stop to oscillate. Considering failure to oscillate as the indicator for VCO's lifetimes, the reliability robustness for two VCO configurations is similar.

V. EVALUATION of DEGRADATION PERFORMANCE of LC-BASED VCO and PMOS-LOADED VCO

Fig. 7 compares the peak-to-peak output voltage, V_{PP}, of two VCOs. The degradation of V_{PP} for PMOS-loaded VCO is decided by the current through MOSFET MB2 and the resistances the VCO load. The bias current decreases significantly such that it dominates V_{PP} reduction. Also, the degradation of V_{PP} for LC-based VCO is caused by current reduction in current-source MB1. When biasing current reduction leads to G_m decrease to less than $2G_{tank}$, the VCO fail to oscillate.

Fig. 8 shows the change in center oscillation frequency of LC-based VCO and PMOS-loaded VCO under different stress conditions. The increase of oscillation frequency for the PMOS-loaded VCO is caused by the increase in bandwidth per gain stage due to decreasing gain; on the other hand, the oscillation frequency for LC-based VCO is decided by the inductor and capacitance values which are relatively independent of transistor characteristics. Therefore the oscillation frequency for PMOS-loaded VCO is more sensitive to operation stress than that of the LC-based VCO.

Fig. 9 shows the comparison of phase noise increase for two VCOs configurations. Under the same supply voltage, the PMOS-loaded VCO increases more than the LC-based VCO.

Fig. 10 shows the comparison the tuning range of LC-based VCO and PMOS-loaded VCO. Tuning range of the PMOS-loaded VCO is determined by the maximum linearity of frequency versus control voltage. If Rss increases, the maximum linearity decreases. Therefore, we observe that the tuning range of PMOS-loaded VCO decreased with stress time. In a LC-based VCO, the tuning range is determined by the size of varactor and its C-V tuning characteristics [9]. From Fig. 10, we observe that when the LC-based VCO with V_{DD} at 4V, its tuning range degrades sharply after 10^6sec. This is due the $|V_{BG}|$ shift causing the varactor bias move from one region to another region [9].

Fig. 11 shows the VCOs' percentage of change in tuning range, V_{PP}, and oscillation frequency in the LC-based VCO configurations. In Fig. 11, LC-based VCO's oscillation frequency is less sensitive to stress voltage, and its percentage of increase only change 2% at 3.83V.

Beyond 3.83V, VCO fail to oscillate. Note that tuning range is most sensitive to operating stress.

For the PMOS-loaded VCO, as shown in Fig. 12, when stressing at 3.8V, oscillation frequency increase almost 10% as a result of its bias current decreased by R_{ss} in the degradation sub-circuit model. V_{PP} degrades first due to operation stress.

Table 1 summarizes the three parameters degradation under stress voltage at 3.5V for ten years.

VI. CONCLUTION

A circuit reliability evaluation and analysis can be achieved through this newly proposed sub-circuit model. Based on this analysis, we conclude that the LC-based VCO has a small percentage of change comparing to the PMOS-loaded VCO except tuning range.

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Parameter Name	Unit	Default Value	Description
R_{SS0}	Ω	4	Flag resistance
K	1/V	-8.70	Voltage-enhanced degradation coefficient
α	—	0.35	Degradation factor
T_C	second	3.83×10^{22}	Characteristic time
R_{GD0}	Ω	4.5×10^{3}	Final breakdown resistance of gate-to-drain
β_1	—	3	Degradation factor
β_2	—	-0.30	Degradation factor
T_{Y0}	Ω	1.67×10^{32}	Initial characteristic time component
T_{S0}	Ω	6.85×10^{38}	Initial characteristic time component
X_S	1/V	-15.01	Voltage-enhanced coefficient
X_V	1/V	-11.81	Voltage-enhanced coefficient

Table 1. Summary of two VCO's percentage of parameter changes under supply voltage 3.5V after ten-year of operation.

Percentage of Change(%)	LC-based VCO	PMOS-loaded VCO
Tuning Range	26%	18%
Output Voltage Peak to Peak	11%	23%
Oscillation Frequency	1%	6%

Table 2. Parameters list of stress model of Rss and R_{GD} resistances.

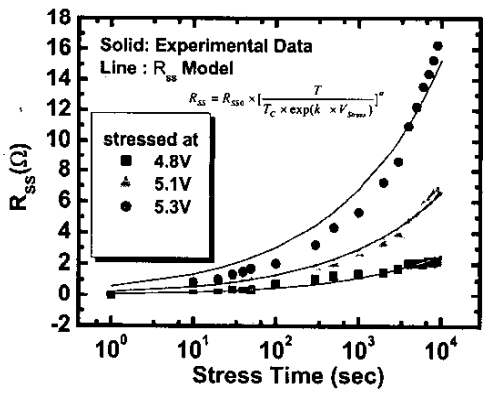

Fig. 2(a). Stress models of Rss resistance obtained from the extracted data points. All parameters are listed in Table 2.

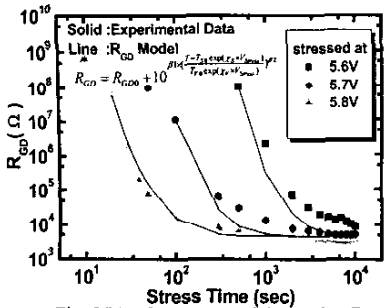

Fig. 2(b). Stress models of R_{GD} resistance obtained from the extracted data points. All parameters are listed in Table 2.

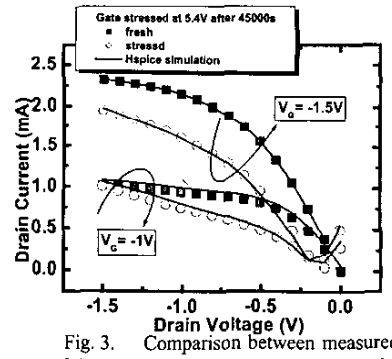

Fig. 3. Comparison between measured I-V and simulated I-V shows that the model can predict transistor performance after stress well. The stress condition on this sample is Vg=5.4V after 45000sec.

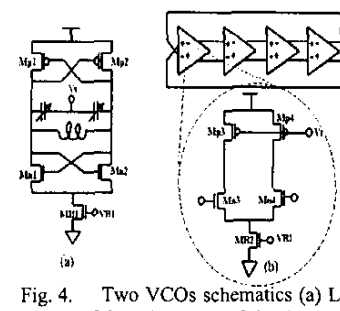

Fig. 4. Two VCOs schematics (a) LC-based VCO and (b) PMOS-loaded VCO use for reliability evaluation.

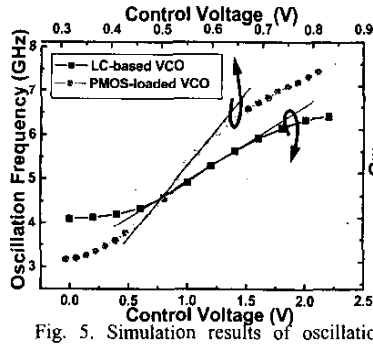

Fig. 5. Simulation results of oscillation frequency versus control voltage of LC-based VCO and PMOS-loaded VCO. PMOS-loaded VCO's tuning range is a slightly wider tuning than that of the LC-tuned VCO.

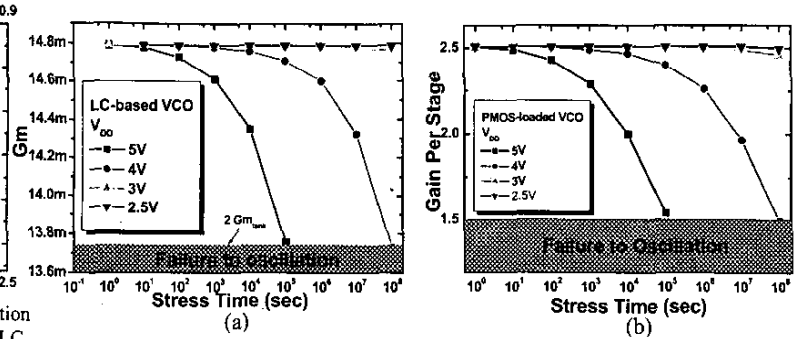

Fig. 6. Simulated failure to oscillation analysis of (a) Gm degradation and (b) gain per stage degradation of LC-based VCO and PMOS-loaded VCO, respectively.

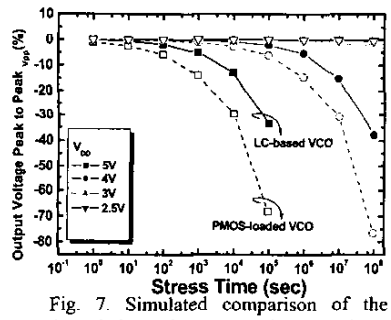

Fig. 7. Simulated comparison of the degradation of output voltage peak to peak between the two VCOs.

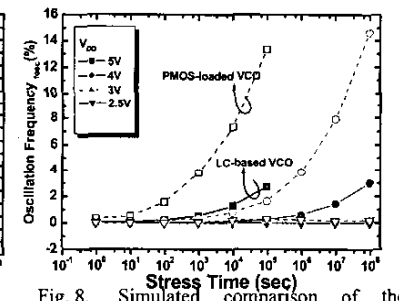

Fig. 8. Simulated comparison of the increase in oscillation frequency between the two VCOs. The center oscillation frequency is 5.2GHz.

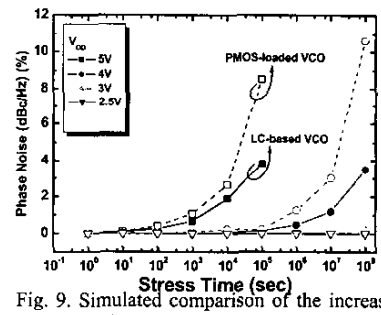

Fig. 9. Simulated comparison of the increase in phase noise between the two VCOs.

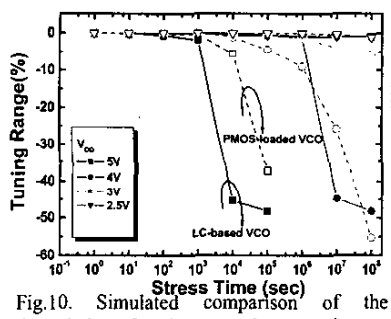

Fig.10. Simulated comparison of the degradation of tuning range between the two VCOs.

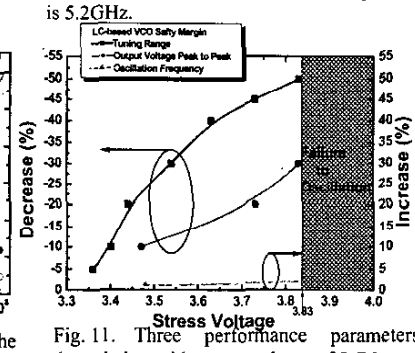

Fig. 11. Three performance parameters degradation with stress voltage of LC-based VCO.

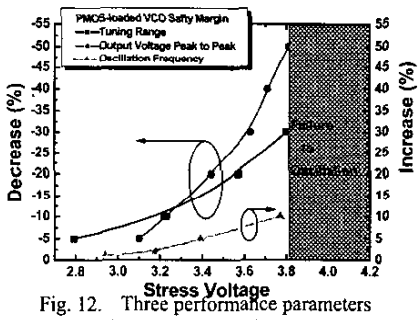

Fig. 12. Three performance parameters degradation with stress voltage of PMOS-loaded VCO.